IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Sunil Kumar Sharma

Title of Invention: **MAPPING OF PROGRAMMABLE LOGIC DEVICES**

Serial No.: 10/675,908

Filing Date: September 29, 2003

Attorney Dkt. No.: 11556(P-54)USA; 2110-80-3

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I hereby certify that this paper is being deposited with the United States Postal Service as First Class Mail and is addressed to Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 4th day of March, 2004.

Jamie Buhl

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97

March 4, 2004

TO THE COMMISSIONER FOR PATENTS:

In compliance with the duty of disclosure under 37 CFR § 1.56, Applicant submits herewith patents, publications, or other information for consideration during the examination of this application.

In accordance with 37 CFR § 1.97, the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made nor that the information cited in the statement is or is considered to be "material" to patentability as defined in 37 CFR § 1.56(b).

_X_ Charge any additional fees to Deposit Account No. 07-1897

_X_ A postcard as acknowledgement of receipt of Form PTO-1449 and copies of the documents cited in the attached form are enclosed.

Respectfully submitted,

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Form PTO-1449 U.S. Department of Commerce (Rev 7-80) PATENT AND TRADEMARK OFFICE LIST OF PRIOR ART CITED BY APPLICANT (Use Several Sheets if necessary)□	Attorney Docket No.: 11556(P-54)USA; 2110-80-3	SERIAL NO. 10/675,908
	APPLICANT: Sunil Kumar Sharma	
	FILING DATE: September 29, 2003	GROUP: 2676

U.S. PATENT DOCUMENTS□

EXAMIER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPLICABLE

FOREIGN PATENT DOCUMENTS□

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)□

		Kuang-Chien Chen, Jason Cong, Yuzheng Ding, Andrew Kahng, Peter Trajmar; *DAG-Map: Graph Based FPGA Technology Mapping For Delay Optimization;* IEEE Design and test of computers, pp 7-20, sept.1992.
		Jason Cong and Yuzheng Ding; *An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup -Table Based FPGA Designs;* IEEE Trans. On Computer Aided Design of Integrated Circuits and Systems CAD, Vol.13, pp 1-12 Jan 1994.
		Jason Cong and Yuzheng Ding; *On Area/Depth Trade-off in LUT-Based FPGA Technology Mapping;* 30th ACM/IEEE design Automation Conference (DAC), pp. 213-218, 1993.
		Jason Cong and Yuzheng Ding; *Beyond the Combinatorial Limit in Depth Minimization for LUT-Based FPGA Designs;* IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 110-114, Nov. 1993.

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw Line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.